A THREE- PHASE SYMMETRICAL DC- LINK MULTILEVEL INVERTER WITH REDUCED NUMBER OF DC SOURCES

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ABSTRACT:

This paper presents a novel three-phase DC-link multilevel inverter topology with reduced number of input DC power supplies. The proposed inverter consists of series-connected half-bridge modules to generate the multilevel waveform and a simple H-bridge module, acting as a polarity generator. The inverter output voltage is transferred to the load through a three-phase transformer, which facilitates a galvanic isolation between the inverter and the load. The proposed topology features many advantages when compared with the conventional multilevel inverters proposed in the literatures. These features include scalability, simple control, reduced number of DC voltage sources and less devices count. A simple sinusoidal pulse-width modulation technique is employed to control the proposed inverter. The performance of the inverter is evaluated under different loading conditions and a comparison with some existing topologies is also presented. The feasibility and effectiveness of the proposed inverter are confirmed through simulation and experimental studies using a scaled down low-voltage laboratory prototype.

Keywords*: Hybrid multilevel inverter, DC-link inverter, half-bridge module, symmetric DC voltage supply, Three- Phase Symmetrical, multilevel inverter technology, High Power Converters.*

INTRODUCTION:

Background

Recently, multilevel inverter technology has become popular in industry for medium and high voltage applications. Hi-Tech industry demands quality electric power that multilevel inverter technology can supply. Multilevel inverter uses number of power semiconductor devices, dc sources batteries/capacitors) to synthesize staircase output voltage waveform. By increasing number of levels the output voltage waveform approaches near to sine wave improving it quality. [1]

MULTILEVEL inverters have received great attention from both academia and industry in the past few decades due to their distinctive features compared to their conventional two-level counterparts [2]. These include, lower switching losses and stress on the semiconductor devices, high quality output waveforms, reduced electromagnetic interference and smaller filtering requirements Cascaded Multilevel Inverters (CMLI) have received special preference in various industrial applications, especially, renewable energy integration. This is particularly because of their modularity and redundancy features along with the absence of complicated capacitor voltage balancing issue, which

is a common problem with other topologies such as diode and capacitor clamped inverters. Several variations of CMLI circuit topology have been documented in the open literature, aiming to increase the attained Voltage levels, which ultimately. [3-6].

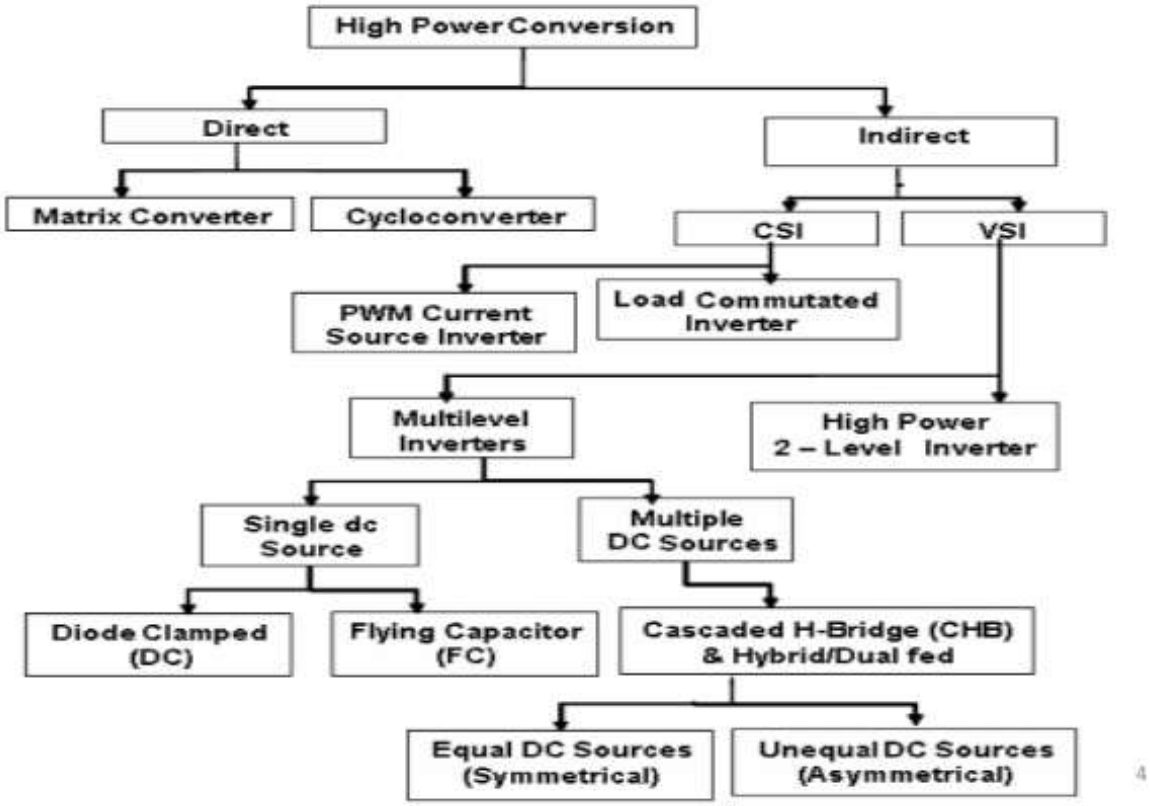


Figure 1: Classification of High-Power Converters

The Proposed Multilevel Inverter and Its Modulation Strategy:

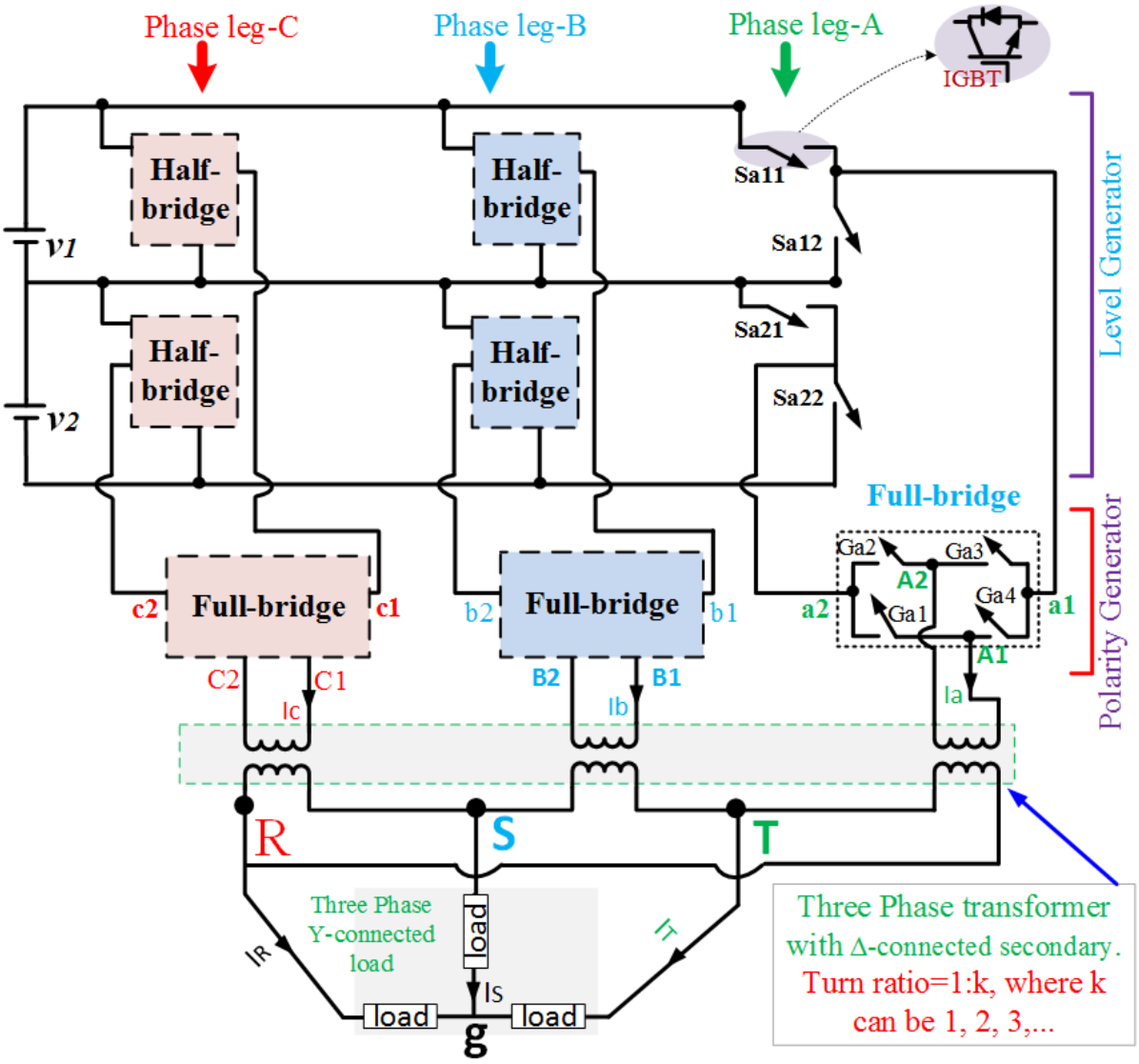


Figure 2: The proposed three-phase CMLI with two half-bridge cells per phase leg

Figure 2 illustrates the proposed CMLI, which consists of two stages. The first stage is a level generator, which generates the unipolar multilevel voltage waveforms by utilizing the cascaded half-bride modules. As shown in Fig. 2, each three half-bridge modules in the three-phase legs-A, B and C are fed from a non-isolated DC power supply. In reality, the DC-power supplies can be battery sources, or rectifier output terminals. Furthermore, the DC supplies can be equally obtained from photovoltaic (PV) output terminals or other renewable energy source. To realize constant output power and voltage for renewable energy sources of intermittent characteristics, some control algorithms such as constant voltage source mode can be employed. It is worth noting that the half-bridge modules will have the same blocking voltage requirement since they are connected across the same DC-supply. This ensures modularity and simple control methods. The second stage is the polarity generator, which utilizes a simple full-bridge inverter to bipolarize the multilevel output voltage waveforms produced by the first stage. [7]

A three-phase transformer couples the outputs of the polarity generator with the load, providing a galvanic isolation as well as boosting to the output voltage. It should be noted that although in Fig. 2 the transformer secondary windings are connected in Δ, it could be also connected in Y, if required. Furthermore, the CMLI presented in Fig. 3 can be easily expanded to generate higher number of levels in the output voltage waveform by adding more half-bridge modules into the level generator. The number of levels, *m* in the output voltage of each polarity generator by utilizing *n*-number of half-bridge modules in each phase leg is given by:

$$m=2n+1 \quad (1)$$

Considering equal input DC voltages (*v1, v2,…,vn*) to the *n*-number of the half-bridge modules in the level generator stage, the input DC voltages can be written as,

$$v1 = v2,\ldots. = vn = VDC; \quad (2)$$

where *VDC* represents a constant value

While the half-bridge modules in the level generator utilize low voltage, high switching frequency devices, the low frequency switches used in the full-bridge modules in the polarity generator experience a voltage stress of a magnitude equals to the summation of the input DC voltage sources [20]. Hence, the voltage stress or standing voltage, *V*pg, stress on the polarity generator switches can be expressed as,

$$V\text{pg, stress} = nVDC \quad (3)$$

It is to be noted that because they are operating at the fundamental switching frequency of 50 Hz, full-bridge modules do not exhibit significant switching losses. On the other side, state-of-the-art technology currently offers switching devices such as Insulated Gate Bipolar Transistors (IGBT)-module, FZ500R65KE3 that can withstand a collector to emitter voltage up to 6.5 kV . Moreover, the operating voltage capacity of the switching devices can be extended by connecting multiple switches in series. A number of CMLIs topologies utilizing half-bridge and H-bridge modules have been implemented for high voltage applications and can be found in the literatures. The rating of the switching devices in the proposed CMLI can be identified according to the voltage requirement of the intended application. It is worth mentioning that as the three-phase transformer is an essential component in the proposed topology, it will inherently fulfill the galvanic isolation requirement for renewable energy grid-connected applications. [8]

SIMULATION AND EXPERIMENTAL RESULTS

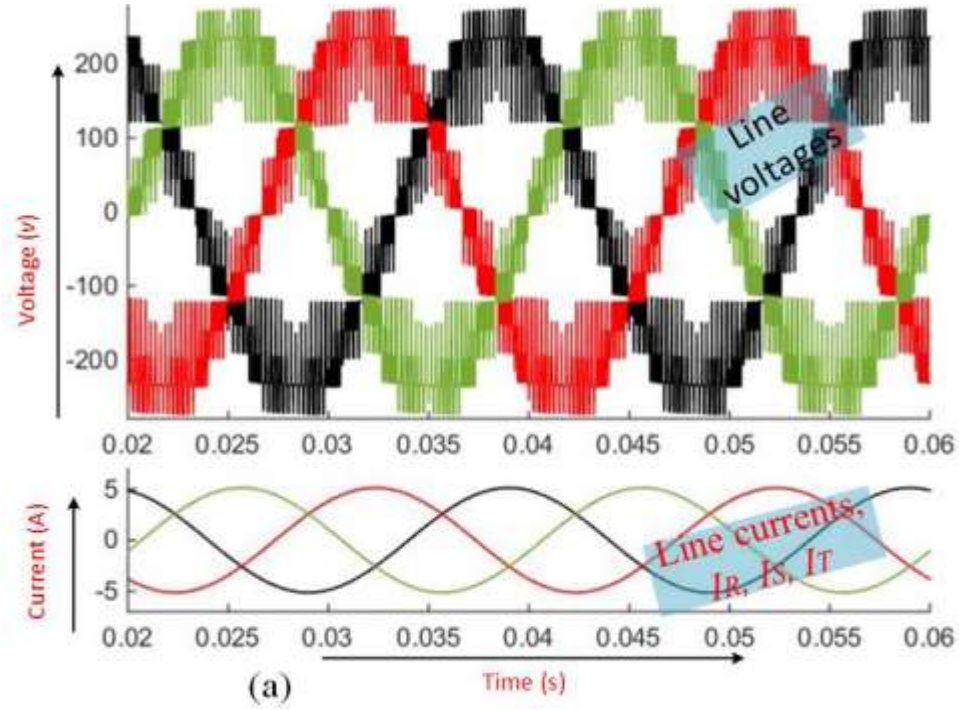
In Figure 3 illustrates the experimental test-rig of the proposed inverter, developed at the Green Electric Energy Park (GEEP), Curtin University. On the other hand, simulation analysis is carried out using the Matlab/Simulink software package. The main parameters of the inverter prototype are

summarized. The input DC voltages from the 'GW Laboratory DC power supplies GPS-3030' are set to provide a constant DC voltage of 60V, i.e. ($v1$=$v2$=60 volts). Both, the level generator and polarity generator stages require twelve IGBTs, each. A digital signal processor (DSP), TMS320F2812 is used to generate the real time switching gate signals. The gate signals from the DSP are connected to the IGBT gates through 24-gate drive circuits. The role of gate drive circuits is to isolate the common ground of the DSP output gate pulses and boost-up their magnitudes to nearly 15 volts. As shown in Fig. 3, there are two printed circuit boards comprising 24-gate drive circuits for the 24 IGBTs in the level generator and polarity generator stages.

In this paper, the conventional SPWM modulation strategy is considered with a carrier frequency of 4kHz for both, simulation and experimental studies. The modulation index Mi is expressed as [9-10].

$$Mi = Am/\ (Np-1)Ac \qquad (4)$$

where *Am* is the magnitude of the reference sine waveform and *Ac* is the magnitude of the carrier signal. Modulation index, *Mi* has an influence on the magnitude of the output line voltages and line currents. The output of the polarity generator is connected to the primary of a three-phase isolation transformer with a turn ratio of 1:1, as shown in Fig. 3.



(a)

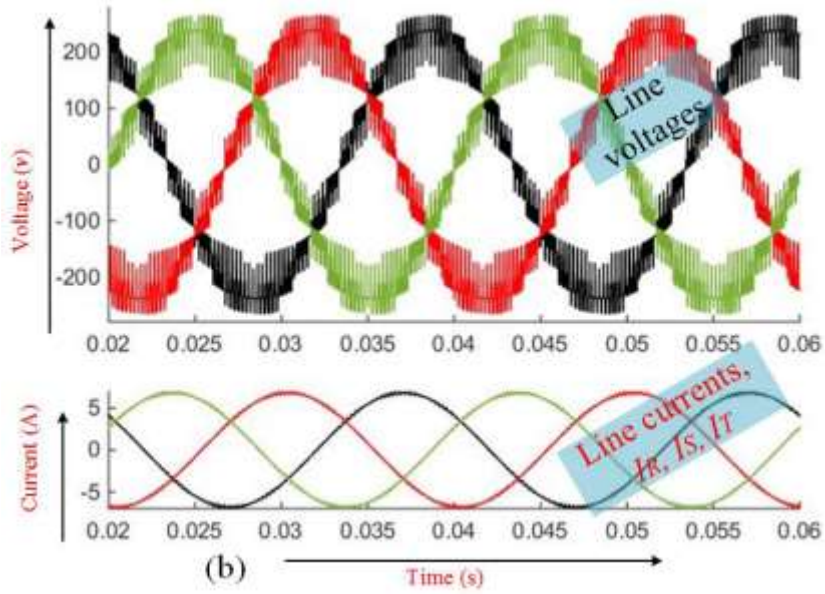


Figure 4: Simulation results of the output line voltages and line currents for (a) load of nearly 0.8– lagging power factor and (b) load of nearly unity power.

As previously mentioned, the secondary side of the transformer can be connected in either Δ or Y. The output line voltages can therefore be presented by (13) or (14) for Δ or Y connection, respectively.

$$\begin{pmatrix} \boldsymbol{VRS} \\ \boldsymbol{VST} \\ \boldsymbol{VTS} \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} \boldsymbol{VC1C2} \\ \boldsymbol{VB1B2} \\ \boldsymbol{VA1A2} \end{pmatrix} \quad \text{.....(5)}$$

$$\begin{pmatrix} \boldsymbol{VRS} \\ \boldsymbol{VST} \\ \boldsymbol{VTS} \end{pmatrix} = \begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{pmatrix} \begin{pmatrix} \boldsymbol{VC1C2} \\ \boldsymbol{VB1B2} \\ \boldsymbol{VA1A2} \end{pmatrix} \quad \text{..... (6)}$$

The performance of the proposed inverter under various loading conditions is assessed as elaborated in the following case studies.

A. Case study 1: The impact of load power factor

Fig. 4 shows the simulation results of the line voltage and line current waveforms of the proposed inverter under load power factor of nearly 0.8 (lagging) and unity power factor, when each phase leg is connected with balanced inductive loads of (20+j15.7Ω) and (20+j1.57Ω), respectively.

On the other hand, Fig 5 illustrate different experimental results for nearly 0.8 lagging and unity power factor loads, respectively. Tektronix TPS2014B digital storage oscilloscope is [11-13]

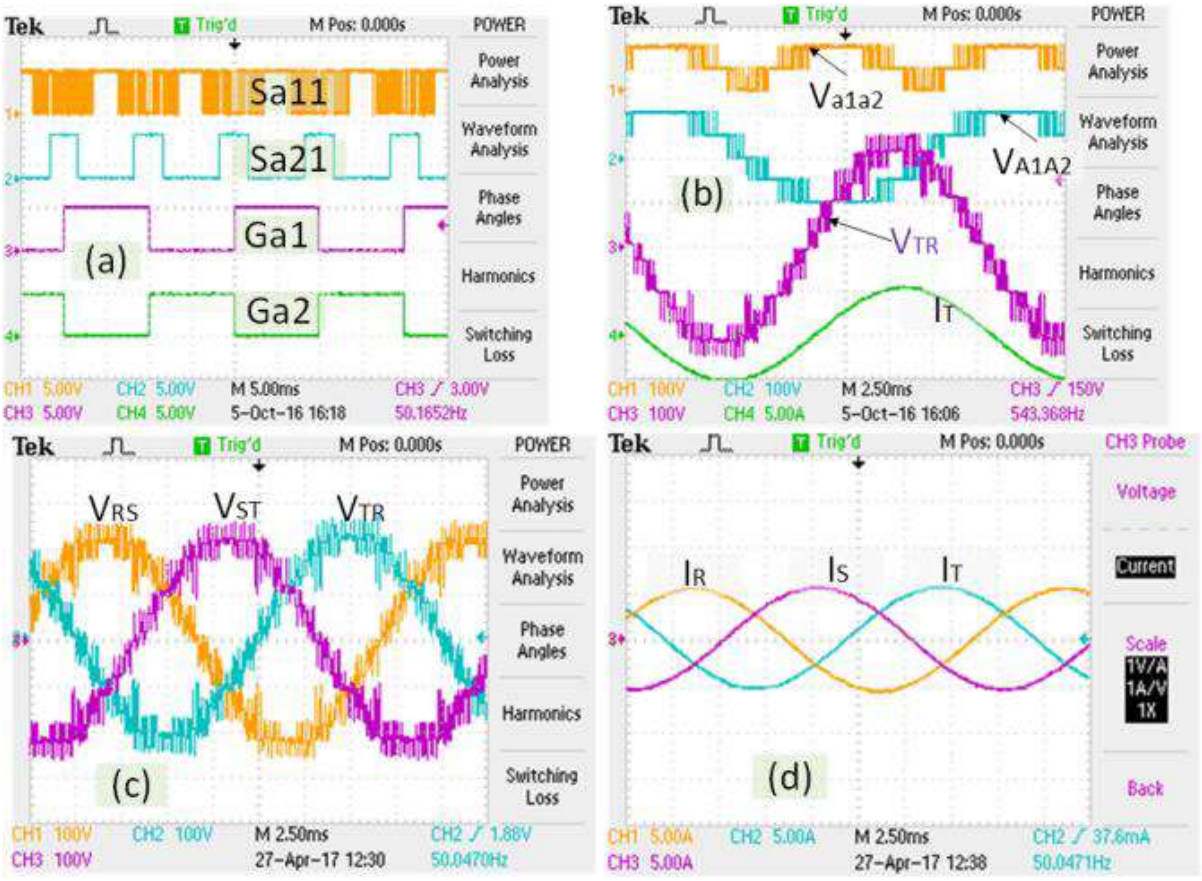


Figure 5: Different experimental results for phase leg-A with a load of nearly 0.8 lagging(a) gate pulses in half-bridge and full bridge module at phase leg-A, (b) level and polarity generator output voltages along with the line voltage and line current for phase leg-A, (c) 3 phase line voltages and (d) 3 phase currents

CONCLUSION:

This paper presents a new symmetrical multilevel inverter topology with two different stages. The proposed inverter requires less power electronic devices and features modularity, hence simple structure, less cost, and high scalability. The number of input DC-supplies for the proposed topology is found to be nearly 67% less than the similar symmetric half-bridge topologies, which is a great achievement for industrial applications. This phenomenon will reduce the complexity of DC voltage management. As being a symmetric structure, all the switching devices experience same voltage stress, which is a very important factor for high voltage applications. The feasibility of the proposed inverter is confirmed through simulation and experimental analysis for different operating conditions.

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